SERIAL I/O BOARD

A B & C

DOCUMENTATION UPDATE

AUGUST 1975

THEORY of OPERATION

88-SIO SERIAL INTERFACE BOARD OPERATION

The serial interface board provides communication between the ALTAIR and any serial Input/Output devices. The board has two device code addresses which are hardware selectable by jumpers for any even numbered address from 0 to 376 (octal). The BAUD rate is also selectable, via jumpers, from 0 through 25,000 BAUD. This board also provides both hardware and software interrupt capability.

Device Select Logic

When the CPU executes an "OUT" or an "IN" instruction, it places the device address (provided with the instruction) on both the 8 lower order address bus lines and the 8 higher order address bus lines.

The 8 lower order address bus lines are fed to the select logic on the board, IC's H & J. If the address on the bus is equal to the address selected on the board, IC I pin 8 will go low, thus enabling IC J pins 3 & 6.

Depending on the state of A0 (the least significant address bit), either the control channel or the data channel will be enabled. If A0 is at a logic low level, IC J pin 4 will go high, thus enabling the control channel. If A0 is at a logic high level, IC J pin 1 will go high, thus enabling the data channel.
Of the two device addresses on the board, the control channel is always an even number and the data channel is always an odd number.

Control Channel

The control channel has two purposes: it is used to enable/disable the hardware interrupt capability for the Input or Output device, and to test the status of the Input/Output device.

After an "IN" instruction is executed with the control channel address, "SINP" goes high and IC J pin 4 is high thus causing IC G pin 3 to go low. This causes IC E pin 13 and IC D pin 8 to go low, thus enabling the Data In lines. (Note that IC D pin 12 is always high except during the initial power on clear, $\overline{POC}$.) $\overline{SWE}$ (Status Word Enable) is always enabled except when inputting data (see Data Channel explanation. This results in the status being inputted to the Data In lines and into the CPU accumulator.

The eight data bits are defined in the chart on the following page.

Bit Definition

DATA BIT	LOGIC LOW LEVEL	LOGIC HIGH LEVEL
7	Output device Ready (X-mitter buffer empty) Also causes a hardware interrupt to occur if interrupt enabled*	Not Ready
6	NOT USED	NOT USED
5	NOT USED	
4		Data Overflow (a new word of data has been recieved before the previous word was inputed to the accumulator)
3		Framming Error (data word has no valid stop bit)
2		Parity Error (recieved parity does not aggree with selected parity)
1	NOT USED	
0	Input device Ready Data is available for computer to input *	NOT READY

When an "OUT" instruction is executed with the control channel address, data bits 0 & 1 are gated through IC's E & A to the Input/Output interrupt flip-flops, IC B.

The chart below describes the result of setting these two bits.

D0	D1	OUTPUT INTERRUPT	INPUT INTERRUPT
low	low	disabled	disabled
low	high	enabled	disabled
high	low	disabled	enabled
high	high	enabled	enabled

As an example: to enable the input device and disable the output device interrupts, load the accumulator with the following:

(X = don't care)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	1

then execute an "OUT" instruction with the control channel address.

Data Channel

The data channel transfers the data between the device and the CPU.

An "OUT" instruction, accompanied by the data channel address (odd numbered address), will pull "SOUT" and IC J pin 1 high, causing IC G pin 11 to go low. As soon as the CPU has put the data from the accumulator onto the data out bus, $\overline{PWR}$ goes low pulling IC S pin 4 low to strobe $\overline{TDS}$ (Transmit Data Strobe) at pin 23 of IC M. This causes the parallel data on the bus to be loaded and then transmitted serially. Pin 4 of IC S also resets the output ready flip-flop (IC F-b) to clear the busy signal to the device.

An "IN" instruction with the data channel address will pull "SINP" and pin 1 of IC J high causing pin 8 of IC G to go low, thus enabling $\overline{RDE}$ (Recieved Data Enable) at pin 4 of IC M and the Data In lines (IC D pin 8). This also disables $\overline{SWE}$ at IC E pin 10. This puts the recieved data on the bus and the CPU strobes it into the accumulator during DBIN (Data Bus In). Pin 8 of IC G also resets the input ready flip-flop (IC F-a) and the UART Data Available flip-flop, $\overline{RDAV}$ at pin 18 of IC M.

UART

The Universal Asynchronous Reciever-Transmitter (UART) provides the paralled to serial and serial to parallel data conversion necessary to interface a serial device with the parallel ALTAIR. It also has a status word for "handshake" and error checking.

Both the Reciever and the Transmitter require a clock input frequency that is 16 times the BAUD rate. This is accomplished with a 12 bit presetable counter (IC's P, Q & R) and a single shot (IC O). If the frequency required is not found in the "BAUD RATE SELECTION CHART" included in this manual, use the formula below:

$$\text{Preset Count Frequency} = 4100 - \left(\frac{\text{Period of Output Frequency (us)}}{.5\text{us}} \right)$$

The maximum frequency is 400KHz. The maximum BAUD rate is (400K/16) 25,000 BAUD.

The UART (IC M) has several programable functions as described below.

UART PIN #	NAME	FUNCTION
35	NPB	Eliminates parity bit from being transmitted when tied high (see pin 39, POE)
36	NSB	When tied low, one stop bit is transmitted When tied high, two stop bits are transmitted
37 38	NDB2 NDB1	Defines the number of data bits per character as shown below:

NDB2	NDB1	# of Bits
low	low	5
low	high	6
high	low	7
high	high	8

39	POE	If NPB is tied low, POE defines whether parity will be odd or even as shown below:

POE	NPB	PARITY	
low	low	odd	
high	low	even	
X	high	none	(X = don't care)

Interrupt

The serial board is provided with hardware interrupt capability. The pads on the board labeled "OUT", "IN" & "BH" are provided for interrupt control. These three pads represent the Output device, the Input device or BotH devices and are jumpered to one or more of the pads labeled "VI" and numbered 0 through 7 at the bottom of the board.

"VI" represents "Vectored Interrupt" and the numbered pads, 0 through 7, are the 8 interrupt lines which connect into the Vectored Interrupt Board (88-VI). The numbers 0 through 7 correspond to the 8 priority levels, with 0 being the lowest and 7 the highest priority.

You can assign the input device and the output device each a different priority, or you can assign both devices a single priority. If you do not have the 88-VI board, you can jumper one of the three pads ("OUT", "IN" & "BH") on one of your I/O boards to the processor input interrupt line.

The processor input interrupt line has a pad labeled "INT" on the board (see assembly manual). This will allow one level of interrupt to the processor. When the interrupt occurs, the processor will immediately jump to the location 70 (octal) and begin execution. Place your interrupt service routine in locations 70 through 77 (octal).

I/O BAUD RATE SELECTION CHART

In the chart below, PRESET COUNT pads 0 through 11 correspond to pads 0 through 11 on the right side of the I/O board. The BAUD rate listed on the left can be obtained by wiring pads 0 through 11 according to the information in the chart; with "+V" for a 1 and "GND" for a 0.

BAUD RATE	PRESET COUNT											
	11	10	9	8	7	6	5	4	3	2	1	0
110	1	0	1	1	1	0	0	1	0	1	0	0
150	1	1	0	0	1	1	0	0	0	0	1	1
300	1	1	1	0	0	1	1	0	0	0	1	1
600	1	1	1	1	0	0	1	1	0	1	0	0
1200	1	1	1	1	1	0	0	1	1	1	0	0
2400	1	1	1	1	1	1	0	1	0	0	0	0
4800	1	1	1	1	1	1	1	0	1	0	1	0
9600	1	1	1	1	1	1	1	1	1	0	0	0
19200	1	1	1	1	1	1	1	1	1	1	1	0

I/O Device Interconnections

The following are available on the 8800 Serial I/O A Board I/O connector:

STSO----Serial Data Output

SRSI----Serial Data Input

GROUND

+5 VOLTS (for power to some external device if necessary)

These signals have the following characteristics:

logic high level = approximately +3 volts

logic low level = approximately -12 volts

There are spaces provided on the ALTAIR back panel for mounting 25-pin connectors. Both male and female connectors are provided with your kit. These connectors and the connections to the device itself are to be made according to the device specifications.

NOTE: The RS-232 standard connections for the 25-pin connectors are as follows:

STSO----Pin 3

SRSI----Pin 2

GROUND----Pin 7

The 25-pin connectors should be "keyed" by clipping pin 4 off on the male connector, and inserting a piece of resistor lead into pin 4 on the female connector.

I/O Device Interconnections

The following signals are available on
the 8800 Serial I/O B Board I/O Connector.

STSO----Serial Data Output

SRSI----Serial Data Input

GROUND

+5 VOLTS--(do not use unless external power is required,
and do not use greater than 100ma.)

There are also several spare pins which are not used.

The signals on this board have the following characteristics:

logic high level = +2v min., +5.5v max.--output current 40ma

logic low level = -1.5v min., +.8v max.--input current 500ua

There are several openings provided in the 8800
Back Panel for interfacing connections to exit
the computer.

The connections to the device itself are to be
made according to the device specifications.

There are spaces provided on the side of the
back panel opposite the transformers for the
mounting of 25-pin connectors. Both male and
female connectors are included with your kit.
These connectors are to be wired according to
the device specifications also.

I/O Device Interconnections

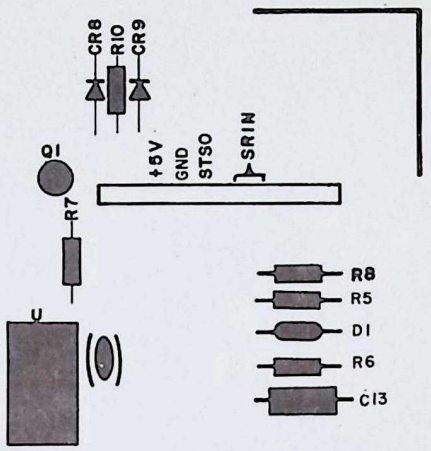
The following are available on the 8800 Serial I/O C Board I/O connector:

STSO----Serial Data Output

SRSI----Serial Data Input (This is indicated on the silk-screen and manual component layouts as "SRIN"; the schematic and theory of operation refer to it as "SRSI".

GROUND

+5 VOLTS (for power to some external device if necessary)



These signals have the following characteristics:

STSO----active = 20ma sink
non-active = high impedance

SRSI----logic high level = greater than 10,000 ohms impedance
logic low level = less than 1,000 ohms impedance

There are spaces provided on the ALTAIR back panel for mounting 25-pin connectors. Both male and female connectors are provided with your kit. These connectors and the connections to the device itself are to be made according to the device specifications. (see TTY INTERCONNECTIONS)

I/O ADDRESS SELECTION CHART

ADDRESS OCTAL	CONNECTIONS I7	I6	I5	I4	I3	I2	I1
000	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
002	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	A1
004	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
006	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2	A1
010	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$	$\overline{A1}$
012	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$	A1
014	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	A2	$\overline{A1}$
016	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	A2	A1
020	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
022	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$	A1
024	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	A2	$\overline{A1}$
026	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	A2	A1
030	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	A3	$\overline{A2}$	$\overline{A1}$
032	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	A3	$\overline{A2}$	A1
034	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	A3	A2	$\overline{A1}$
036	$\overline{A7}$	$\overline{A6}$	$\overline{A5}$	A4	A3	A2	A1
040	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
042	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	A1
044	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
046	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	A2	A1
050	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	A3	$\overline{A2}$	$\overline{A1}$
052	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	A3	$\overline{A2}$	A1
054	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	A3	A2	$\overline{A1}$
056	$\overline{A7}$	$\overline{A6}$	A5	$\overline{A4}$	A3	A2	A1
060	$\overline{A7}$	$\overline{A6}$	A5	A4	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$

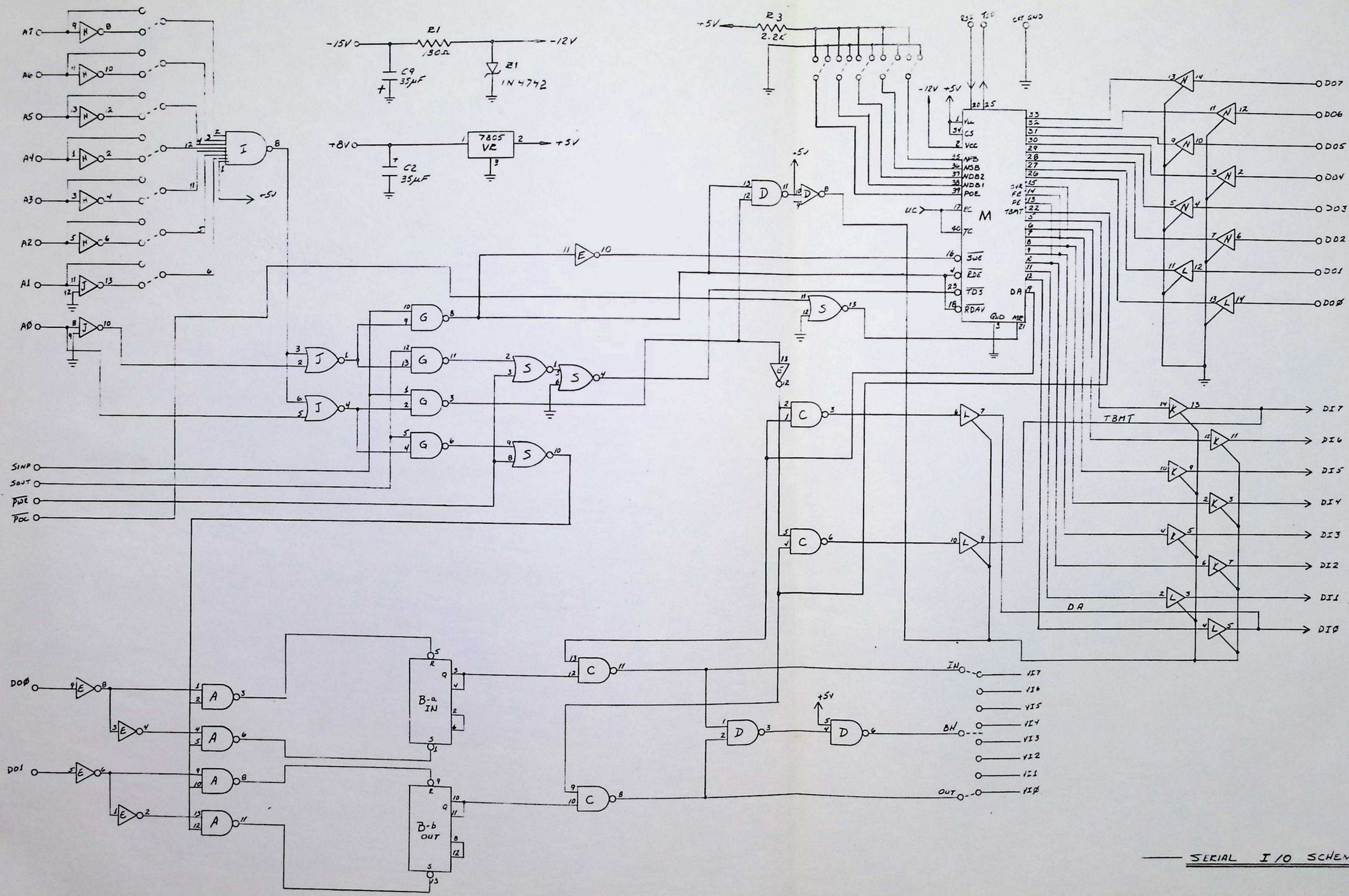
ADDRESS OCTAL	CONNECTIONS I7	I6	I5	I4	I3	I2	I1
062	$\overline{A7}$	$\overline{A6}$	A5	A4	$\overline{A3}$	$\overline{A2}$	A1
064	$\overline{A7}$	$\overline{A6}$	A5	A4	$\overline{A3}$	A2	$\overline{A1}$
066	$\overline{A7}$	$\overline{A6}$	A5	A4	$\overline{A3}$	A2	A1
070	$\overline{A7}$	$\overline{A6}$	A5	A4	A3	$\overline{A2}$	$\overline{A1}$
072	$\overline{A7}$	$\overline{A6}$	A5	A4	A3	$\overline{A2}$	A1
074	$\overline{A7}$	$\overline{A6}$	A5	A4	A3	A2	$\overline{A1}$
076	$\overline{A7}$	$\overline{A6}$	A5	A4	A3	A2	A1
100	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
102	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	A1
104	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
106	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2	A1
110	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$	$\overline{A1}$
112	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$	A1
114	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	A3	A2	$\overline{A1}$
116	$\overline{A7}$	A6	$\overline{A5}$	$\overline{A4}$	A3	A2	A1
120	$\overline{A7}$	A6	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
122	$\overline{A7}$	A6	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$	A1
124	$\overline{A7}$	A6	$\overline{A5}$	A4	$\overline{A3}$	A2	$\overline{A1}$
126	$\overline{A7}$	A6	$\overline{A5}$	A4	$\overline{A3}$	A2	A1
130	$\overline{A7}$	A6	$\overline{A5}$	A4	A3	$\overline{A2}$	$\overline{A1}$
132	$\overline{A7}$	A6	$\overline{A5}$	A4	A3	$\overline{A2}$	A1
134	$\overline{A7}$	A6	$\overline{A5}$	A4	A3	A2	$\overline{A1}$
136	$\overline{A7}$	A6	$\overline{A5}$	A4	A3	A2	A1
140	$\overline{A7}$	A6	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
142	$\overline{A7}$	A6	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	A1

ADDRESS OCTAL	CONNECTIONS I7	I6	I5	I4	I3	I2	I1
144	$\overline{A7}$	A6	A5	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
146	$\overline{A7}$	A6	A5	$\overline{A4}$	$\overline{A3}$	A2	A1
150	$\overline{A7}$	A6	A5	$\overline{A4}$	A3	$\overline{A2}$	$\overline{A1}$
152	$\overline{A7}$	A6	A5	$\overline{A4}$	A3	$\overline{A2}$	A1
154	$\overline{A7}$	A6	A5	$\overline{A4}$	A3	A2	$\overline{A1}$
156	$\overline{A7}$	A6	A5	$\overline{A4}$	A3	A2	A1
160	$\overline{A7}$	A6	A5	A4	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
162	$\overline{A7}$	A6	A5	A4	$\overline{A3}$	$\overline{A2}$	A1
164	$\overline{A7}$	A6	A5	A4	$\overline{A3}$	A2	$\overline{A1}$
166	$\overline{A7}$	A6	A5	A4	$\overline{A3}$	A2	A1
170	$\overline{A7}$	A6	A5	A4	A3	$\overline{A2}$	$\overline{A1}$
172	$\overline{A7}$	A6	A5	A4	A3	$\overline{A2}$	A1
174	$\overline{A7}$	A6	A5	A4	A3	A2	$\overline{A1}$
176	$\overline{A7}$	A6	A5	A4	A3	A2	A1
200	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
202	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	A1
204	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
206	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2	A1
210	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$	$\overline{A1}$
212	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$	A1
214	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	A2	$\overline{A1}$
216	A7	$\overline{A6}$	$\overline{A5}$	$\overline{A4}$	A3	A2	A1
220	A7	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
222	A7	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$	A1
224	A7	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	A2	$\overline{A1}$

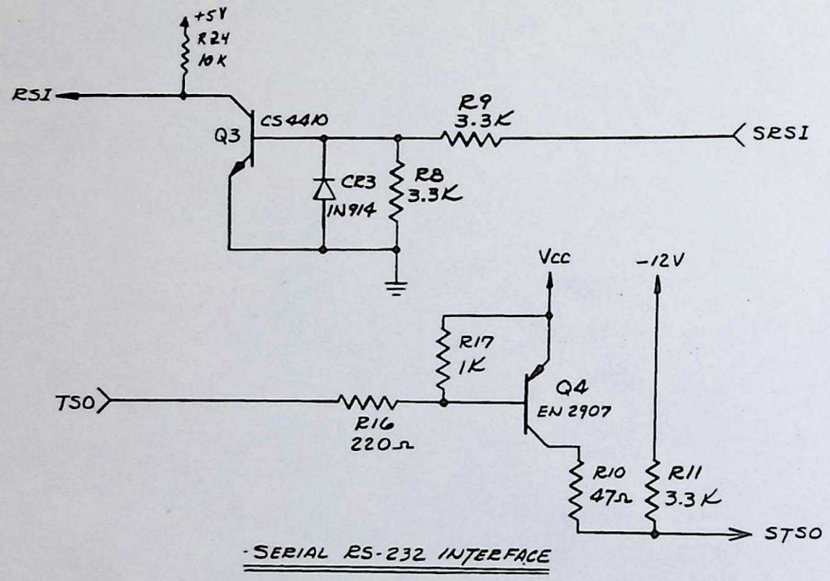
ADDRESS OCTAL	CONNECTIONS I7	I6	I5	I4	I3	I2	I1
226	A7	$\overline{A6}$	$\overline{A5}$	A4	$\overline{A3}$	A2	A1
230	A7	$\overline{A6}$	$\overline{A5}$	A4	A3	$\overline{A2}$	$\overline{A1}$
232	A7	$\overline{A6}$	$\overline{A5}$	A4	A3	$\overline{A2}$	A1
234	A7	$\overline{A6}$	$\overline{A5}$	A4	A3	A2	$\overline{A1}$
236	A7	$\overline{A6}$	$\overline{A5}$	A4	A3	A2	A1
240	A7	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
242	A7	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	A1
244	A7	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
246	A7	$\overline{A6}$	A5	$\overline{A4}$	$\overline{A3}$	A2	A1
250	A7	$\overline{A6}$	A5	$\overline{A4}$	A3	$\overline{A2}$	$\overline{A1}$
252	A7	$\overline{A6}$	A5	$\overline{A4}$	A3	$\overline{A2}$	A1
254	A7	$\overline{A6}$	A5	$\overline{A4}$	A3	A2	$\overline{A1}$
256	A7	$\overline{A6}$	A5	$\overline{A4}$	A3	A2	A1
260	A7	$\overline{A6}$	A5	A4	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
262	A7	$\overline{A6}$	A5	A4	$\overline{A3}$	$\overline{A2}$	A1
264	A7	$\overline{A6}$	A5	A4	$\overline{A3}$	A2	$\overline{A1}$
266	A7	$\overline{A6}$	A5	A4	$\overline{A3}$	A2	A1
270	A7	$\overline{A6}$	A5	A4	A3	$\overline{A2}$	$\overline{A1}$
272	A7	$\overline{A6}$	A5	A4	A3	$\overline{A2}$	A1
274	A7	$\overline{A6}$	A5	A4	A3	A2	$\overline{A1}$
276	A7	$\overline{A6}$	A5	A4	A3	A2	A1
300	A7	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
302	A7	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	A1
304	A7	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
306	A7	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2	A1

ADDRESS OCTAL	CONNECTIONS I7	I6	I5	I4	I3	I2	I1
310	A7	A6	$\overline{A5}$	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
312	A7	A6	$\overline{A5}$	$\overline{A4}$	A3	$\overline{A2}$	A1
314	A7	A6	$\overline{A5}$	$\overline{A4}$	A3	A2	$\overline{A1}$
316	A7	A6	$\overline{A5}$	$\overline{A4}$	A3	A2	A1
320	A7	A6	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
322	A7	A6	$\overline{A5}$	A4	$\overline{A3}$	$\overline{A2}$	A1
324	A7	A6	$\overline{A5}$	A4	$\overline{A3}$	A2	$\overline{A1}$
326	A7	A6	$\overline{A5}$	A4	$\overline{A3}$	A2	A1
330	A7	A6	$\overline{A5}$	A4	A3	$\overline{A2}$	$\overline{A1}$
332	A7	A6	$\overline{A5}$	A4	A3	$\overline{A2}$	A1
334	A7	A6	$\overline{A5}$	A4	A3	A2	$\overline{A1}$
336	A7	A6	$\overline{A5}$	A4	A3	A2	A1
340	A7	A6	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
342	A7	A6	A5	$\overline{A4}$	$\overline{A3}$	$\overline{A2}$	A1
344	A7	A6	A5	$\overline{A4}$	$\overline{A3}$	A2	$\overline{A1}$
346	A7	A6	A5	$\overline{A4}$	$\overline{A3}$	A2	A1
350	A7	A6	A5	$\overline{A4}$	A3	$\overline{A2}$	$\overline{A1}$
352	A7	A6	A5	$\overline{A4}$	A3	$\overline{A2}$	A1
354	A7	A6	A5	$\overline{A4}$	A3	A2	$\overline{A1}$
356	A7	A6	A5	$\overline{A4}$	A3	A2	A1
360	A7	A6	A5	A4	$\overline{A3}$	$\overline{A2}$	$\overline{A1}$
362	A7	A6	A5	A4	$\overline{A3}$	$\overline{A2}$	A1
364	A7	A6	A5	A4	$\overline{A3}$	A2	$\overline{A1}$
366	A7	A6	A5	A4	$\overline{A3}$	A2	A1
370	A7	A6	A5	A4	A3	$\overline{A2}$	$\overline{A1}$

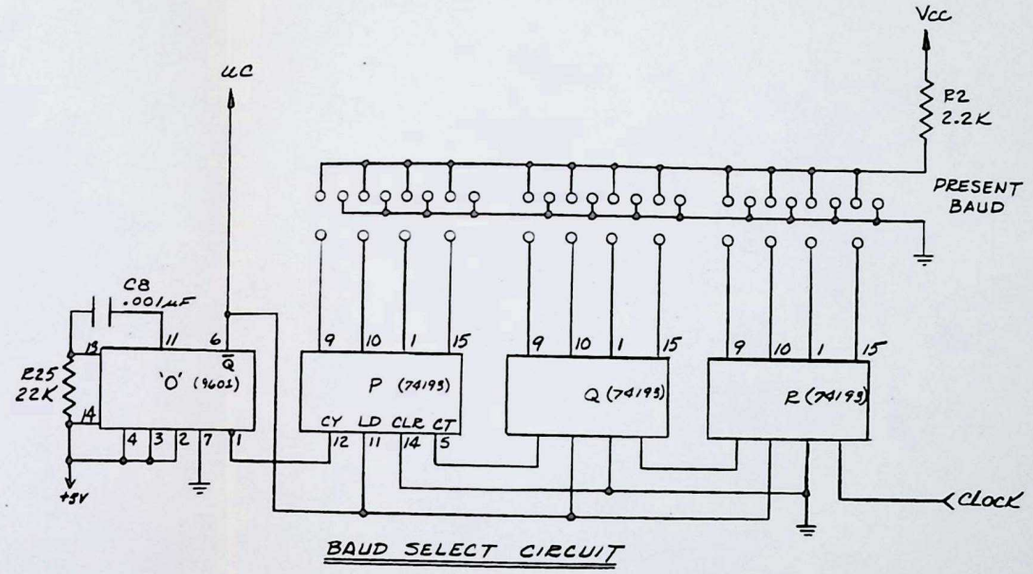
ADDRESS OCTAL	CONNECTIONS						
	I7	I6	I5	I4	I3	I2	I1
372	A7	A6	A5	A4	A3	$\overline{A2}$	A1
374	A7	A6	A5	A4	A3	A2	$\overline{A1}$
376	A7	A6	A5	A4	A3	A2	A1



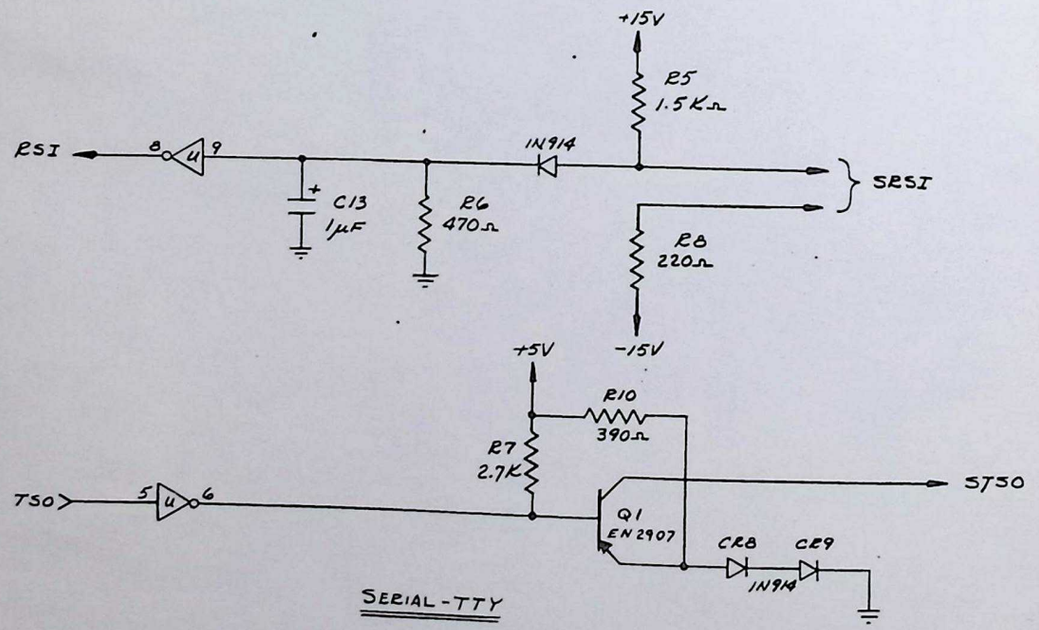
SERIAL I/O SCHEMATIC



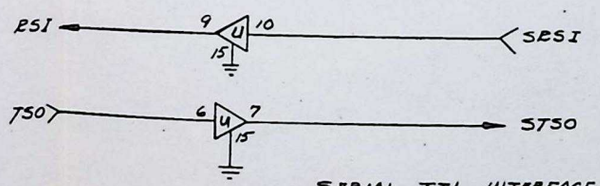
SERIAL RS-232 INTERFACE



BAUD SELECT CIRCUIT



SERIAL-TTY



SERIAL TTL INTERFACE